

COMPOUND TRANSISTOR

on-chip resistor PNP silicon epitaxial transistor For mid-speed switching

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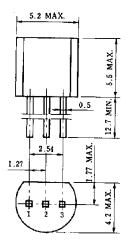
FEATURES

- On-chip bias resistor (R₁ = 22 kΩ)
- Complementary transistor with AA1A4Z

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Symbol	Ratings	Unit
Vсво	-60	V
VCEO	-50	V
Vebo	-5	V
IC(DC)	-100	mA
IC(pulse) *	-200	mA
Рт	250	mW
Tj	150	
Tstg	–55 to +150	°C
	VCBO VCEO VEBO IC(DC) IC(pulse) * PT Tj	V -60 V -60 V -50 V -50 Ic(DC) -100 Ic(pulse) * -200 PT 250 Tj 150

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

PACKAGE DRAWING (UNIT: mm)



Electrode Connection 1. Emitter EIAJ : SC~43B 2. Collector JEDEC : TO 92

3. Base IEC PA33

* PW \leq 10 ms, duty cycle \leq 50 %

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	Ісво	$V_{CB} = -50 \text{ V}, \text{ I}_{E} = 0$			-100	nA
DC current gain	hfe1 **	$V_{CE} = -5.0 \text{ V}, \text{ Ic} = -5.0 \text{ mA}$	135	280	600	-
DC current gain	hFE2 **	$V_{CE} = -5.0 \text{ V}, \text{ Ic} = -50 \text{ mA}$	100	200		-
Collector saturation voltage	V _{CE(sat)} **	$I_{C} = -5.0 \text{ mA}, I_{B} = -0.25 \text{ mA}$		-0.06	-0.2	V
Low level input voltage	VIL **	$V_{CE} = -5.0 \text{ V}, \text{ Ic} = -100 \ \mu\text{A}$		-0.57	-0.5	V
High level input voltage	VIH **	$V_{CE} = -0.2 \text{ V}, \text{ Ic} = -5.0 \text{ mA}$	-3.0	-1.1		V
Input resistance	R1		15.4	22	28.6	kΩ
Turn-on time	ton	$V_{\text{CC}} = -5.0 \text{ V}, \text{ R}_{\text{L}} = 1.0 \text{ k}\Omega$			0.2	μs
Storage time	tstg	$V_{I} = -5.0 V$, PW = 2.0 μ s			5.0	μs
Turn-off time	t _{off}	duty cycle≤2 %			6.0	μs

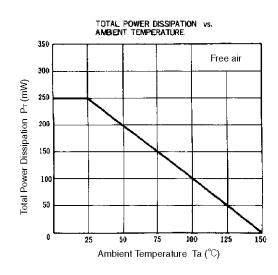
** Pulse test PW \leq 350 μ s, duty cycle \leq 2 %

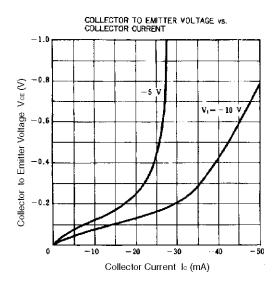
hfe CLASSIFICATION

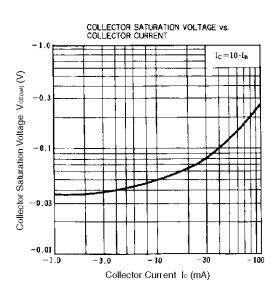
Marking	Q	Р	К
hfe1	135 to 270	200 to 400	300 to 600

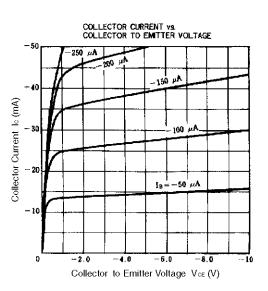
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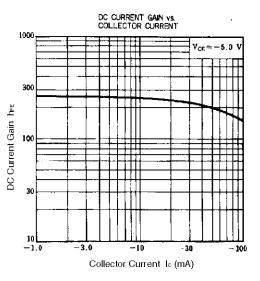
TYPICAL CHARACTERISTICS (Ta = 25°C)

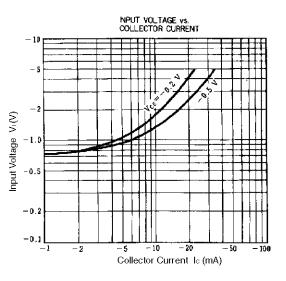


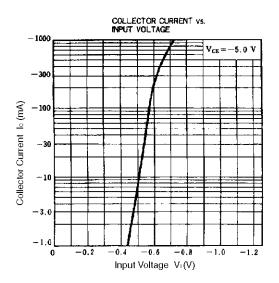


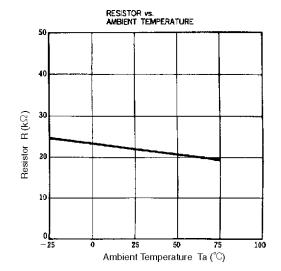












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